

● PRINTER RUSH ●
(PTO ASSISTANCE)

Application : 09/138146 Examiner : Clark GAU : 2815

From: MR Location: IDC FMF FDC Date: 04-28-05

Tracking #: EPM09138146 Week Date: 04/18/05

DOC CODE	DOC DATE	MISCELLANEOUS
<input type="checkbox"/> 1449	_____	<input type="checkbox"/> Continuing Data
<input type="checkbox"/> IDS	_____	<input type="checkbox"/> Foreign Priority
<input checked="" type="checkbox"/> CLM	_____	<input type="checkbox"/> Document Legibility
<input type="checkbox"/> IIFW	_____	<input type="checkbox"/> Fees
<input type="checkbox"/> SRFW	_____	<input type="checkbox"/> Other
<input type="checkbox"/> DRW	_____	
<input type="checkbox"/> OATH	_____	
<input type="checkbox"/> 312	_____	
<input type="checkbox"/> SPEC	_____	

[RUSH] MESSAGE: Claim 2 is if line has a description
for claim dependency but the number is
not listed.
Please provide the number for dependency.

Thank you,
RR

[XRUSH] RESPONSE: Corrected. Claim 2 depends from
claim 1. See attached page.

INITIALS: DG

NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.
REV 10/04

IN THE CLAIMS:

1. (Currently Amended) A chip carrier comprising:
a base having a surface and a periphery;
an inner well having a periphery extending along the periphery of the base and wherein
the inner well has a second base having a second depth between the second base and the surface;
an outer well extending along the periphery of the inner well, and wherein the outer well
has a first base having a first depth between the first base and the surface, wherein the first depth
is greater than the second depth.

DGO
7-1-05

2. (Currently Amended) The chip carrier according to claim 1 wherein the first inner
well and the second outer well form a flexible structure.

3. (Original) The chip carrier according to claim 1 wherein the outer well includes an
outer wall and an inner wall and the inner well includes an outer wall coupled to the inner wall of
the outer well.

Kindly cancel Claim 4 without prejudice or disclaimer

5. (Previously Presented) The chip carrier according to claim 1 further comprising an
integrated circuit removably positioned on the base.